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Design and Implementation of MAC Unit Using ANT Fixed Width Replica Redundancy Block

B.Shivalakshmi[1] , B.J .Prem Prasanna Kumar[2]

PG Scholar, Dept. of ECE SWEC, Hyderabad, TS, India

Associate Professor, Dept. of ECE, SWEC, Hyderabad, TS, India

ABSTRACT: MAC (multiplier accumulator unit) is the hardware unit . The MAC consists of multiplier adder, and accumulator. The MAC (multiplier accumulate unit) unit is used in digital signal processing (DSP) applications. MAC unit is operation is multiply and addition functions . MAC have two stages , first stage is performs product of the given number and the result is forward the second stage. that is addition and accumulate .it stages are executed the single round . There is lot of research operation on MAC implementation and it can be give the comparative performance .

KEYWORDS: Multiplier Accumulator Unit(MAC), Digital Signal Processing (DSP), Algorithmic Noise Tolerant (ANT) **,** Replica Redundancy Block (RPR) **.**

I. INTRODUCTION

Multiplier accumulator unit (MAC) used in the is an unavoidable part in various automated flag getting ready (DSP) applications including enlargements as well as social events. Multiplier accumulate unit is used for world class propelled sign getting ready systems. The DSP applications fuse isolating, convolution, and internal things[1].
controller for the various applications.The multiplier accumulator unit (MAC) used in large number of digital signal processing (DSP) application .it is used in improve signal processing ability .MAC are used in the micro controller for the various applications.that are the servo audio control MAC is execution unit of the processor implementation .

Figure 1. Multiplier Accumulator Unit (MAC)

The MAC unit consists of three blocks .that are the multiplier ,adder and accumulator. Power dissipation is one of the most important design in integrated circuits, and also speed is also most important in integrated circuit. high speed and low power MAC unit is necessary for any DSP processor. that is because of speed is always the concern DSP systems [2]. It is mainly used in DSP systems .In MAC unit consists the multiplier, adder ,and accumulator .multiplier which done the multiplication ,adder to do the addition of values and that values stored the in accumulator .In accumulator stored the one bit extra value that is carry bit .

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II. OVER VIEW OF THE PROJECT

The application like optical correspondence systems which relies up on DSP . The Fast Fourier Transform (FFT) in like manner requires development and growth. A MAC unit involves a multiplier and a gather containing the total of the past dynamic things. The diagram includes 16 bit ANT (algorithmic noise tolerant) fixed width RPR (replica redundancy) multiplier and 32 bit of sparse kogge-stone adder and accumulator. And we also compare vedic multiplier of MAC is also design. A plan of elite 16 bit Multiplier-and-Accumulator (MAC) is actualized in this paper. MAC unit performs important operation in huge numbers of the computerized flag handling (DSP) applications. The aggregate outline is coded with verilog-HDL and the union is finished utilizing Cadence RTL complier utilizing regular libraries . MAC unit is an unavoidable segment in numerous advanced flag preparing (DSP) applications including duplications or potentially gatherings. MAC unit is utilized for superior advanced flag handling frameworks. The DSP applications incorporate separating, convolution, and internal items. The greater part of computerized flag preparing techniques utilize nonlinear capacities, for example, discrete cosine change (DCT) or discrete wavelet changes (DWT). Since they are fundamentally proficient by dreary utilization of increase and expansion, the speed of the duplication and expansion number decides the execution speed and execution of the whole count .

III. EXISTING PROJECT

The Area Efficient Multiplier Design Using Fixed-Width Replica Redundancy by embracing algorithmic noise tolerant (ANT) engineering with the settled width multiplier to assemble the decreased accuracy imitation excess piece (RPR). The proposed ANT engineering can take care of the demand of high exactness, low power utilization, and zone productivity In this paper, proposed An Area Efficient Multiplier Design Using Fixed-Width Replica. We plan the settled width RPR with blunder pay circuit by means of dissecting of likelihood and measurements. Utilizing the incomplete item terms of info adjustment vector and minor input redress vector to bring down the truncation blunders, the equipment intricacy of mistake pay circuit can be disentangled. In a 16 × 16 bit ANT multiplier, circuit zone in our settled width RPR can be lower and power utilization in our ANT configuration.Fast development of versatile and remote figuring frameworks as of late drives the requirement for ultralow control frameworks. To bring down the power dispersal, supply voltage scaling [6] is broadly utilized as a compelling low-control strategy since the power utilization in CMOS circuits is corresponding to the square of supply voltage. Be that as it may, in profound sub-micrometer process advances, commotion impedance issues have raised trouble to outline the solid and productive microelectronics frameworks; consequently, the plan procedures to improve clamor resilience have been broadly created [7]-[8]. A forceful low-control procedure, alluded to as voltage over scaling (VOS), was proposed in bring down supply voltage past basic supply voltage without yielding the throughput. In any case, VOS prompts extreme corruption in motion to-commotion proportion signal to noise ratio (SNR). A novel algorithmic noise tolerant (ANT) strategy joined VOS primary square with decreased accuracy reproduction (RPR), which battles delicate blunders viably while accomplishing significant vitality sparing. Some ANT Miss sharpening plans are displayed in [9]-[10] the ANT outline idea is additionally reached out to framework level. In any case, the RPR outlines in the ANT are in a tweaked way, which are not effectively received and rehashed. The RPR outlines in the ANT plans can work in a quick way, however their equipment intricacy is excessively unpredictable as appeared in Fig.1. Accordingly, the RPR outline in the ANT configuration is as yet the most prominent plan due to its effortlessness. Be that as it may, receiving with RPR should at present pay additional region overhead and power utilization. In this paper, we additionally proposed a simple way utilizing the settled width RPR to supplant the full-width RPR square. Utilizing the settled width RPR, the calculation mistake can be revised with bring down power utilization and lower zone overhead. We take utilization of likelihood, insights, and fractional item weight investigation to locate the estimated pay vector for a more exact RPR outline. All together not to build the basic way delay, we confine the pay circuit in RPR must not be situated in the basic way. Therefore, we can understand the ANT outline with littler circuit territory, bring down power utilization, and lower basic supply.

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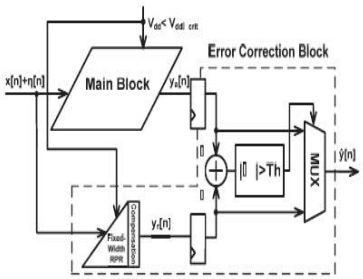

Figure 2. ANT architecture fixed width multiplier

ANT multiplier design using fixed width RPR In this paper, we additionally proposed the settled fixed width RPR (replica redundancy) tore put the full-width RPR hinder in the ANT (algorithmic noise tolerant)plan [2],as appeared in Fig.2, which can not just give higher calculation accuracy, bring down power utilization, and lower territory overhead in RPR, yet in addition perform with higher SNR, more region productive, bring down working sup-handle voltage, and bring down power utilization in understanding the ANT design. We exhibit our settled width RPR-based ANT outline in an ANT multiplier. The settled width outlines are typically connected in DSP applications to maintain a strategic distance from boundless development of bit width. Cutting off n-bit minimum significant piece (LSB) yield is a well known answer for develop a settled width DSP with n-bit info and n-bit yield. The equipment many-sided quality and power utilization of a settled width DSP is for the most part about portion of the full-length one. Be that as it may, truncation of LSB part brings about adjusting mistake, which should be remunerated decisively. Numerous literary works have been introduced to diminish the truncation mistake with constant amendment esteem with variable rectification esteem. The circuit intricacy to repay with constant revised esteem can be less complex than that of variable redress esteem; be that as it may, the variable adjustment approaches are generally more exact, their remuneration technique is to remunerate the truncation mistake between the full-length multiplier and the settled width multiplier. In any case, in the settled width RPR of an ANT multiplier, the remuneration mistake we have to redress is the general truncation blunder of MDSP square. Not at all like, our remuneration strategy is to repay the truncation blunder between the full-length MDSP multiplier and the settled width RPR multiplier.

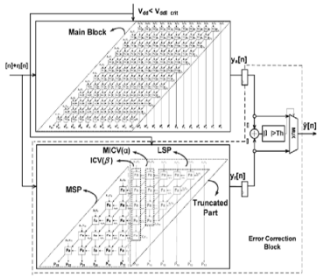

Figure 3. ANT architecture with fixed width RPR .

In these days, there are many settled width multiplier outlines connected to the full-width multipliers. Nonetheless, there is still no settled width RPR configuration connected to the ANT multiplier plans. To accomplish more exact blunder remuneration, we repay the truncation mistake with variable adjustment esteem. We develop the blunder remuneration circuit principally utilizing the halfway item terms with the biggest weight at all significant fragment. The blunder pay calculation makes utilization of likelihood, measurements, and straight relapse investigation to locate the estimated pay esteem [16]. To spare equipment unpredictability, the pay vector in the incomplete item terms with the biggest weight at all significant section is specifically infuse into the settled width RPR, which does not require

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additional remuneration rationale entryways [17]. To additionally bring down the remuneration blunder, we likewise consider the impact of truncated items with the second most significant bits on the mistake pay. We propose a mistake remuneration circuit utilizing a basic minor info rectification vector to pay the blunder remained. All together not to build the basic way delay, we find the pay circuit in the non-basic way of the settled width RPR. As contrasted and the full-width RPR outline in [15], the proposed settled width RPR multiplier performs with higher SNR as well as with bring down hardware range and lower control utilization. A Proposed Precise Error Compensation Vector for Fixed Width RPR Design In the ANT plan, the capacity of RPR is to rectify the blunders happening in the yield of MDSP and keep up the SNR of entire framework while bringing down supply voltage. On account of utilizing settled width RPR to acknowledge ANT design, went just lower circuit range and power utilization, yet additionally quicken the calculation speed as contrasted and the regular full-length RPR. Be that as it may, we have to repay gigantic truncation mistake because of cutting off numerous equipment components in the LSB part of MDSP. In the MDSP of n-bit ANT Baugh– Woolley cluster multiplier, its two unsigned n-bit contributions of X and Y can be communicated as he (n/2)-bit unsigned full-width Baugh– Woolley incomplete item exhibit can be partitioned into four subsets, which are most significant part (MSP), input adjustment vector [ICV(ß)].

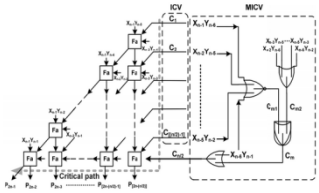

Figure 4. Proposed high-accuracy fixed-width RPR multiplier with compensation constructed by the multiple truncation error correction vectors combined ICV together.

IV. PROPOSED PROJECT

4.1 16*16 BIT ANT FIXED WIDTH RPR MULTIPLIER

16*16 bit ANT fixed width RPR multiplier is based on the 12*12 bit ANT fixed width RPR multiplier .The full adders and half adders used in this design is the baugh-wooley multiplier. In 16 *16 bit ANT fixed width RPR multiplier compensate the truncation error by the help of variable correction value . we construct the error compensation circuit using partial product terms. It is used in the linear regression analysis to find the approximate compensation value. The ANT fixed width RPR multiplier design we use the full adders and half adders 240 full adders and 15 half adders.

4.2 32 BIT SPARSE KOGGESTONE ADDER

32 bit sparse kogge stone adder is have the functionality parallel prefix adder and Parallel prefix adder is used speed up logic operation of the system. Implementation of parallel prefix adder structure in vlsi have effective performs .the different types of parallel prefix adder in technology . sparse kogge stone adder is the sub type of koggestone adder. Sparse koggestone is the fastest adder architecture . sparse kogge stone adder have the block cells and grey cells . And it cells compared with the koggestone adder ..and its added to the final sum is calculated by ripple carry adder . It sparse koggestone is decreases the critical path delay and it is increased the speed and verifying the synthesis report it is observed that it requires [11]. it's Are reconfigurable logic as field programmable gate arrays has gaining in quality in recent years as a result of it offers improve performance and speed , power over DSP – based microprocessor . It are used in DSP and telecommunications applications in big reduction development time and price over application specific computer circuit styles . It's are used movable mobile phones For example the sparse koggestone adder is in diagrametic representation . its are the four bit kogge stone adder .

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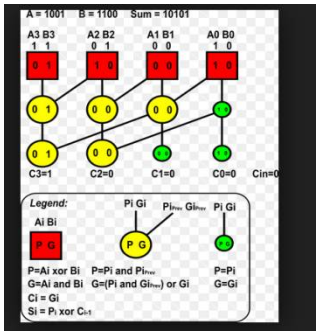

Figure 5. Sparse kogee stone adder

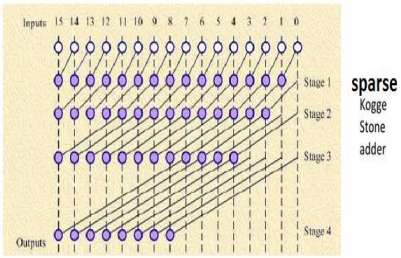

Figure 6. Diagramatic representation of sparse koggestone adder .

4.3 MAC ACCUMULATOR

MAC accumulator is the bit of 33 accumulator .it's is store the results of partial product by on adder .it is a one type of register , and the bit extra is carry bit . Since MAC (Multiplier and Accumulator) portion can be reconfigured to give each one of the four encourages parameters for any of the two sidebands, there are 3 techniques for operation of the correlate.

• Non-polar mode : To gage one and just of the two polarization RR or LL with the full band information. • Indian-Polar mode . For the estimation of the total power nourish I on non enraptured source. The estimation of both the polarization RR and LL per sideband is possible, however gives 128 channels of a similar polarization giving confined assurance. This is in a general sense used for continuum observations.

• Polar mode : To gage all the four encourages parameters using either upper or lower sideband which experiences both sidebands of the correlate. In this mode each MAC unit gives two or three RR, LL or LL, LR having 33 piece unearthly channels for each mix.(ll,rr,rl,lr) is the values of circular polarization values .

Specially sparse kogge -stone adder designed for the ANT fixed width RPR multiplier and the 24*24 bit of ANT fixed width replica redundancy block multipliers is design .due to this the area power time delay and complexity decreases .By doing these we are get the comparison values to higher bit rate.

4.4 VEDIC MULTIPLIER ACCUMULATOR UNIT

Vedic multipliers is the one type of multiplier which is occupy the more area , power , complexity by compares to the ANT (algorithmic noise tolerant) fixed width replica redundancy (RPR) multiplier . In vedic MAC we are used the 32 bit sparse koggestone adder [12]. .Its are partial products send to the accumulator .accumulator is a register.

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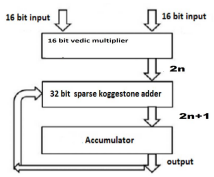

Figure .7. Vedic multiplier accumulate unit

V. RESULTS

Figure.10. Simulation of output of 16 bit ANT fixed width replica redundancy block of multiplier accumulator in native compiler .

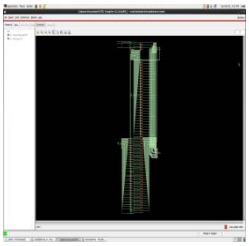

Figure.11. 16 bit ANT fixed width replica redundancy block of multiplier accumulator in register level complier

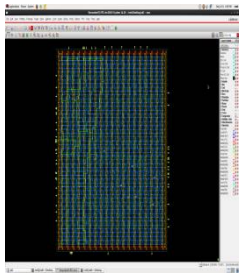

Figure.12. 16 bit ANT fixed width replica redundancy block of multiplier accumulator in physical design .

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VI. CONCLUSION

The MAC unit improves the low power application it is improves the switching activity of CMOS VLSI circuits. the MAC unit help reduction of power ,area in the system. MAC unit improve signal to noise ratio. it is decreases the replica values of the system.MAC unit is implemented in TSMA 90-nm process. The MAC unit is to identify the improved architecture. The ANT multiplier has been developed to reduce the number of partial product . multiplier MAC unit is used in the DSP application. Real time applications like mobile phones and video coding. It is used in the digital wavelet transforms.. it is used in in fast Fourier transforms and medical equipment .

VII. FUTURE SCOPE

The power savings may increases the following criteria is considered in the future low power VLSI design. Number of bits considered may increased the encoding scheme . Power area can be reduced by improving the partial product compression ratio. Lower the power and area power is decreases in vlsi systems is a big problem , so multiplier accumulator unit decreases the area and power .in many real time, applications we used in the multiplier accumulator unit.

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BIOGRAPHY

Ms. B.Shiva Lakshmi has completed B.E in ECE Department from Maheswara Engineering college, Patancheru, Hyderabad. Presently pursuing Masters in VLSI System Design in Sridevi Women‟s Engineering College, Vattina-gulapally, Gandipet, Hyderabad, India.

Mr. B.J.Prem Prasanna Kumar, presently working as Associate professor in SWEC(Hyderabad) Telangana. He is pursuing his Ph.d from Sridevi Women's Engineering College. He is having 18 years of teaching experience.